What is claimed is:

1. A method for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic elements entered for use in a designing process, comprising:

setting one or more conditions satisfied by a route to be distinguished from other routes from the starting point pin to the end point pin; and

distinguishing a route from others depending on whether or not the route satisfies the set condition, and carrying out a search for a route from the starting point pin to the end point pin on each route to be distinguished from others by a condition.

2. The method according to claim 1, wherein

when there are a plurality of the same type of routes to be distinguished from others, one of the plurality of routes is selected and set aside according to predetermined selection rules.

3. The method according to claim 1, wherein

a route can be distinguished from others based

on a type of condition, a number of conditions, or a combination of conditions.

4. The method according to claim 1, wherein

said search for a route is carried out by generating at least data indicating a pin positioned immediately before, and a route identification code for identification of a route while passing control forward pin by pin from the starting point pin; and

a value of the route identification code is first set at least after the condition is satisfied to distinguish the route from others by the condition.

5. The method according to claim 4, wherein

said route is selected according to the selection rules that the same route identification code is assigned.

6. A method for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic devices entered for use in a designing process, comprising:

when there are two or more routes from the starting point pin to the end point pin joining one another on the same pin, setting one or more conditions to be satisfied among the two or more routes when one of the two or more routes is selected; and

carrying out a search for a route from the starting point pin to the end point pin while selecting and setting aside only one of the two or more routes satisfying the set condition.

7. The method according to claim 6, wherein

a route having a longest or shortest delay time is selected from two or more routes satisfying the condition.

8. The method according to claim 6, wherein

said starting point pin is a clock source outputting an externally input or internally generated clock signal.

9. The method according to claim 8, wherein

said condition includes the clock source immediately before a joint pin matching in the two or more routes, and the same phase in transmission

of a clock signal from the clock source.

10. The method according to claim 7, wherein

when a path connecting the pins has the longest delay time and the shortest delay time, and the path having the longest delay time is selected from among the two or more routes satisfying the condition, the condition includes the relationship in which the delay time of a section, from a pin on which the two or more routes branch to the junction pin immediately after the branch pin, computed using the shortest delay time of a path in one of the two or more routes is equal to or longer than the delay time of the section computed using the longest delay time of the path of another route of the two or more routes.

11. The method according to claim 7, wherein

when a path connecting the pins has the longest delay time and the shortest delay time, and the path having the shortest delay time is selected from among the two or more routes satisfying the condition, the condition includes the relationship in which the delay time of a section, from a pin on which the two or more routes branch to the junction

pin immediately after the branch pin, computed using the longest delay time of a path in one of the two or more routes is equal to or shorter than the delay time of the section computed using the shortest delay time of the path of another route of the two or more routes.

12. The method according to claim 7, wherein

when a path connecting the pins has the longest delay time and the shortest delay time, and the path having the longest delay time is selected from among the two or more routes satisfying the condition, the condition includes the relationship in which the delay time of a section, from a pin on which the two or more routes branch to the junction pin immediately after the branch pin, computed using the shortest delay time of a path from the branch pin to another branch pin immediately before the junction pin in one of the two or more routes, and using the longest delay time of a path from the other branch pin to the junction pin is equal to or longer than the delay time of the section computed using the longest delay time of the path of another route of the two or more routes.

13. The method according to claim 7, wherein

when a path connecting the pins has the longest delay time and the shortest delay time, and the path having the shortest delay time is selected from among the two or more routes satisfying the condition, the condition includes the relationship in which the delay time of a section, from a pin on which the two or more routes branch to the junction pin immediately after the branch pin, computed using the longest delay time of a path from the branch pin to another branch pin immediately before the junction pin in one of the two or more routes, and using the shortest delay time of a path from the other branch pin to the junction pin is equal to or shorter than the delay time of the section computed using the shortest delay time of the path of another route of the two or more routes.

14. The method according to claim 8, wherein

said search for a route is carried out by generating at least data indicating a pin positioned immediately before, and a route identification code for identification of a route while passing control forward pin by pin from the starting point pin; and

a value of the route identification code is first set at least after control is passed beyond a pin which is a clock source other than the starting point pin.

15. The method according to claim 14, wherein said condition includes the route identification codes match each other.

16. A method for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic devices entered for use in a designing process, comprising:

when there are two or more routes joining one another on the same joint pin in routes from the starting point pin to the end point pin, setting one or more conditions to be satisfied among the two or more routes when the two or more routes are synthesized; and

carrying out a search for a route from the starting point pin to the end point pin while synthesizing two or more routes satisfying the set condition into one route.

17. The method according to claim 16, wherein

said search for a route is carried out by generating at least data indicating a pin positioned immediately before each pin, and analysis information for use in performing a waveform analysis on the signal while passing control forward pin by pin from the starting point pin to the end point pin; and

synthesizing two or more routes satisfying the set condition is performed by joining the analysis information respectively generated in the two or more routes.

18. The method according to claim 16, wherein

when the starting point pin is a clock source outputting an externally input or internally generated clock signal, the condition includes matching clock sources positioned immediately before the joint pin among the two or more routes, and the same phase of the clock signal from the clock sources.

19. The method according to claim 17, wherein

said analysis information includes at least data indicating a phase in transmission of a clock

signal from a clock source immediately before, and delay data for computation of a pulse width of the clock signal.

20. The method according to claim 19, wherein:

when a path connecting the pins has a longest delay time and a shortest delay time, and a phase in transmission of the clock signal is the same as a phase of the pin positioned immediately before, at least one of a delay difference of a starting point computed by subtracting a shortest delay time from a longest delay time required to transmit the clock signal from rise to rise of the clock signal; a delay difference of an end point computed by subtracting a shortest delay time required to transmit the clock signal from fall to fall of the clock signal from a longest delay time required to transmit the clock signal from rise to rise of the clock signal; a third delay difference computed by subtracting a shortest delay time required to transmit the clock signal from rise to rise of the clock signal from a longest delay time required to transmit the clock signal from fall to fall of the clock signal; and a fourth delay difference computed by subtracting a shortest delay time from

a longest delay time required to transmit the clock signal from fall to fall of the clock signal is computed as a delay difference from the pin immediately before;

said delay data has one or more total delay differences containing one of the starting through fourth delay differences to be added; and

said delay data is generated by adding the delay difference computed using one of the starting point through fourth delay differences to a total delay difference among the delay data generated on the pin positioned immediately before.

21. The method according to claim 19, wherein:

when a path connecting the pins has a longest delay time and a shortest delay time, and a phase in transmission of the clock signal is opposite the phase of the pin positioned immediately before, at least one of a fifth delay difference computed by subtracting a shortest delay time from a longest delay time required to transmit the clock signal from fall to rise of the clock signal; a sixth delay difference computed by subtracting a shortest delay time required to transmit the clock signal from rise to fall of the clock signal from a

longest delay time required to transmit the clock signal from fall to rise of the clock signal; a seventh delay difference computed by subtracting a shortest delay time required to transmit the clock signal from fall to rise of the clock signal from a longest delay time required to transmit the clock signal from rise to fall of the clock signal; and an eighth delay difference computed by subtracting a shortest delay time from a longest delay time required to transmit the clock signal from rise to fall of the clock signal is computed as a delay difference from the pin immediately before;

said delay data has one or more total delay differences containing one of the fifth through eighth delay differences to be added; and

said delay data is generated by adding the delay difference computed using one of the fifth through eighth delay differences to a total delay difference among the delay data generated on the pin positioned immediately before.

22. The method according to claim 20 or 21, wherein

said two or more routes satisfying the set condition are synthesized by selecting the largest

delay difference or the shortest delay difference by type of delay difference generated as the delay data in the two or more routes.

23. The method according to claim 19, wherein

when a pin positioned immediately before a pin for which the analysis information is generated is a clock source other than the starting point pin, the data indicating the phase is inphase data, and a value of the total delay difference forming the delay data is a predetermined initial value.

24. A method for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic devices entered for use in a designing process, comprising:

when there are two or more routes from the starting point pin to the end point pin joining one another on the same pin, setting one or more conditions to be satisfied among the two or more routes when the two or more routes are synthesized into one route;

confirming whether or not two or more routes satisfying the set condition join one another on

each pin while passing control forward pin by pin from the starting point pin; and

when it is certain by the confirming step that two or more routes satisfying the set condition join one another, selecting and setting aside one of the two or more routes, and carrying out a search for a route from the starting point pin to the end point pin.

25. A method for use in carrying out a timing analysis for verification of an operation of an electronic circuit designed by combining cells which are basic devices entered in advance for a designing process, comprising:

extracting a data route for use in the timing analysis by searching for a data route for transmission of a data signal in the electronic circuit while distinguishing a route from others depending on whether or not the route satisfies a first condition group comprising one or more predetermined conditions;

extracting a clock route for use in the timing analysis by searching for a clock route for transmission of a clock signal while selecting and setting aside one of two or more clock routes

joining on the same pin among clock routes for transmission of the clock signal in the electronic circuit depending on whether or not a second condition group formed by one or more predetermined conditions is satisfied; and

carrying out the timing analysis on each combination of the extracted data route and the clock route.

26. A method for use in carrying out a waveform analysis for verification of an operation of an electronic circuit designed by combining cells which are basic devices entered in advance for a designing process, comprising:

extracting a clock signal for use in the waveform analysis by joining two or more clock routes on the same junction pin in transmitting the clock signal in the electronic circuit, and by searching for a clock route for transmission of a clock signal while generating analysis information on each pin for use in performing the waveform analysis on the clock signal depending on whether or not one or more predetermined conditions are satisfied; and

carrying out a waveform analysis for

confirming a pulse width of a clock signal transmitted through the clock route according to the analysis information generated in the extracted clock route.

27. An apparatus for use in carrying out a simulation for verification of an operation of an electronic circuit designed by combining cells which are basic devices entered in advance for a designing process, comprising:

a first route data obtaining unit obtaining route data indicating a data route extracted by searching for a data route for transmission of a data signal in the electronic circuit while distinguishing a route from others depending on whether or not the route satisfies a first condition group comprising one or more predetermined conditions;

a second route data obtaining unit obtaining route data indicating a clock route extracted by searching for a clock route for transmission of a clock signal while selecting and setting aside one of two or more clock routes joining on the same pin among clock routes for transmission of the clock signal in the electronic circuit depending on

whether or not a second condition formed by one or more predetermined conditions is satisfied; and

a simulation unit carrying out a timing analysis for verification of the operation using route data obtained by said first and second route data obtaining units.

28. An apparatus for use in carrying out a simulation for verification of an operation of an electronic circuit designed by combining cells which are basic devices entered in advance for a designing process, comprising:

a route data obtaining unit obtaining route data indicating an extracted clock route by searching for a clock route for transmission of a clock signal while synthesizing two or more clock routes on the same junction pin in transmitting the clock signal in the electronic circuit, and generating analysis information on each pin for use in performing the waveform analysis on the clock signal depending on whether or not one or more predetermined conditions are satisfied; and

a simulation unit performing a waveform analysis for confirmation of a pulse width of the clock signal according to analysis information

about a pin indicated by the route data obtained by said route data obtaining unit.

29. A storage medium storing a program executed by a route search apparatus for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic devices entered for use in a designing process, comprising the functions of:

setting one or more conditions satisfied by a route to be distinguished from other routes from the starting point pin to the end point pin; and

distinguishing a route from others depending on whether or not the route satisfies the set condition, and carrying out a search for a route from the starting point pin to the end point pin on each route to be distinguished from others by a condition.

30. A storage medium storing a program executed by a route search apparatus for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by

combining cells which are basic devices entered for use in a designing process, comprising the functions of:

when there are two or more routes from the starting point pin to the end point pin joining one another on the same pin, setting one or more conditions to be satisfied among the two or more routes when one of the two or more routes is selected; and

carrying out a search for a route from the starting point pin to the end point pin while selecting and setting aside only one of the two or more routes satisfying the set condition.

31. A storage medium storing a program executed by a route search apparatus for a search for a route of a signal from a starting point pin to an end point pin in an electronic circuit designed by combining cells which are basic devices entered for use in a designing process, comprising the functions of:

when there are two or more routes synthesizing one another on the same joint pin in routes from the starting point pin to the end point pin, setting one or more conditions to be satisfied

among the two or more routes when the two or more routes are synthesized; and

carrying out a search for a route from the starting point pin to the end point pin while synthesizing two or more routes satisfying the set condition into one route.

32. A method for a search for a route from a starting point to an end point comprising:

setting one or more conditions satisfied by a route to be distinguished from other routes from the starting point to the end point; and

distinguishing a route from others depending on whether or not the route satisfies the set condition, and carrying out a search for a route from the starting point to the end point on each route to be distinguished from others by a condition.